



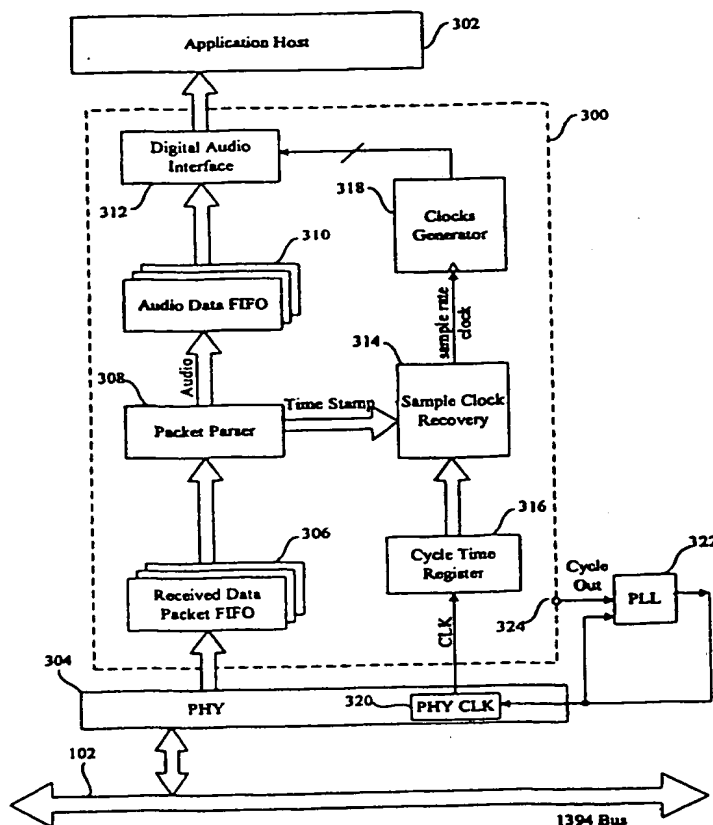
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(54) Title: METHOD AND APPARATUS FOR LOW JITTER CLOCK RECOVERY

(57) Abstract

A method and apparatus is described for reducing jitter in data sample clock rates recovered from isochronous streams of data packets having associated time stamp values, such as in an IEEE 1394 bus-interconnected system. Jitter associated with variations in the free running quartz-driven PHY clocks is reduced by instead driving local PHY clocks with a phase-locked loop circuit referenced to the Link cycle-out pin, which toggles when the cycle time register cycle-offset field wraps and the cycle-count field increments. Because the cycle-out pin toggles at a frequency proportional to the cycle master's PHY clock, jitter associated with local PHY clock variations is reduced. Jitter associated with quantization noise from finite length time stamp generation is reduced by dithering and noise shape filtering conventional time stamps. This decorrelates the jitter and shifts the associated noise out of the expected frequency band of the sample clock signal to be recovered.



METHOD AND APPARATUS FOR LOW JITTER CLOCK RECOVERY

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The present invention relates generally to bus system architecture and, more particularly, to a method and apparatus for reducing jitter in isochronous communications clock recovery.

10 BACKGROUND

Today's consumer electronic devices are increasingly being implemented as special-purpose computer systems, complete with processor, memory, and I/O functionality. The various companies who design and manufacture these devices may have their own particular interconnect technology and
15 communication protocols. Consequently, compatibility problems can occur when connecting devices made by different manufacturers. In home entertainment systems, for example, a DVD player manufactured by one company may be incompatible with an audio speaker subsystem manufactured by another company.

To facilitate today's increasingly complex communication between
20 electronic devices, various standards have been developed. In particular, the IEEE 1394 standard for a High Performance Serial Bus (also known as the "FireWire" bus) has been established to facilitate the development of compatible consumer electronics devices. In addition to defining a standard bus communications protocol, the FireWire bus architecture also provides for standard connections, with each
25 interconnected device being able to communicate with every other such device without requiring individual point-to-point connections between the various devices.

The IEEE 1394 standard (IEEE 1394-1995 and IEEE 1394a supplement) is entitled "Standard for a High Performance Serial Bus," and is based on the ISO/IEC 13213 (ANSI/IEEE 1212) specification, entitled "Information technology—Microprocessor systems—Control and Status Registers (CSR) Architecture for microcomputer
5 buses."

Referring to Figure 1, a typical home entertainment system 100 is depicted. The system includes a high speed bus, such as an IEEE 1394 bus 102, that interconnects a variety of electronic devices. The particular configuration depicted is intended solely to show the functional interconnection of representative devices.
10 Those skilled in the art understand that FireWire bus architecture supports tree and daisy chain connection configurations.

A DVD player 104 is included for playing DVD disks and correspondingly outputting audio and MPEG video data streams on the 1394 bus 102. The audio and video data streams are transported over isochronous channels of the
15 1394 bus 102, with a surround sound decoder 106 receiving the audio data stream and a video decoder/monitor 108 receiving the MPEG video data stream. A cable or satellite set-top box 110 receives media from a cable or satellite television provider and outputs corresponding audio and MPEG video data streams on isochronous channels of the 1394 bus 102. The surround decoder 106 receives the audio data, and
20 the video decoder/monitor 108 receives the video data.

The surround sound decoder 106 receives compressed audio signals from other devices connected to the 1394 Bus 102 and decodes the audio. The decoded audio data is then output on the 1394 bus 102 to an amplifier/speaker subsystem 112. The video decoder/monitor 108 decodes MPEG data streams
25 received from various video source devices on the 1394 bus 102. Once decoded, the

uncompressed video signal is then typically output to a video monitor for presentation.

A controller 114 provides a point of control for all devices in the system 100. The controller 114 may also provide a user interface to configure the system when various devices are added or removed. The controller typically includes a user interface for adjusting audio volume, turning devices on and off, selecting channels on the set-top box 110, etc. Indeed, the controller may be the only device a user interacts with (other than inserting disks into the DVD player 104).

Each of the interconnected devices shown in the system 100 Figure 1 includes interface circuitry connecting the 1394 Bus 102 to the particular application circuitry included in the devices. Such interface circuitry includes both the physical electrical connections (known as the PHY layer) and the data format translation interface (known as the Link layer). Such interface circuitry is well known for those skilled in the art, and the general features of such circuitry need not be described herein.

For video and audio applications, which require constant data transfer rates, it is particularly important that a device receiving such data accurately recover the sample rate clock signal from the device transmitting such data. This ensures that data buffers in the system do not overflow or underflow. FireWire bus architecture supports transmission of isochronous data packets including time stamp information that can be used to recover the sample rate clock, such as in accordance with the IEC 61883 standard, entitled "Digital Interface for Consumer Audio/Video Equipment." Because there is no requirement that different data streams be frequency related (i.e., isochronous streams may have free-running sample rates), each receiving device or node must implement a separate clock recovery circuit for each received isochronous channel of the 1394 bus.

Referring to Figure 2, a functional block diagram depicts the prior art approach of providing time stamps and correspondingly recovering a sample rate clock. The interface circuitry included within a transmitting device or node 200 is depicted, as is a portion of the interface circuitry included within the receiving device or node 202. The transmitting node 200 includes a latch 204 that latches a lower portion of the value stored in a cycle time register 206 included within the Link layer of the interface circuitry. The latch 204 latches the cycle time value every predetermined number of cycles of the sample rate clock (such as a digital audio word clock in the case of audio data transmission). A transfer delay value is added to the latched cycle time register value, and the resulting time stamp is inserted into the header of the corresponding isochronous data packet 208. As is known to those skilled in the art, the value of the transfer delay is determined at system initialization or bus reset.

At the receiving device or node 202, the received time stamp is compared with the corresponding lower portion of the value stored in the receiving node's cycle time register 210. A comparator 212 produces a pulse signal in the event of equality, which is then input to a phase-locked loop (PLL) circuit 214 to recover the sample rate clock signal. All cycle time registers in a 1394 bus-based system are periodically set (at nominal 125 μ s intervals) to the same value by a cycle start command issued by the cycle master node, as is well understood in the art. Each node's cycle time register is then incremented by a quartz driven clock circuit included in the PHY layer of each node, with each clock circuit producing a nominal 24.576 MHz clock signal. Figure 2 depicts PHY clock circuits 216 and 218 of the transmitting node 200 and receiving node 202, respectively.

The above-described approach of generating and receiving time stamps has two particular problems associated with jitter. The first problem is that the separate PHY clock circuits included in each node may have slightly different

frequencies. The IEEE 1394 standard limits frequency deviations to 100 ppm from the nominal rate. Thus, the PHY clocks 216, 218 of the transmitting and receiving nodes 200, 202 could be off from one another by as much as 200 ppm. Over the 125 μ s isochronous cycle time, this translates to

5 $(200) \cdot (24.576 \text{ s}^{-1}) \cdot (125 \mu\text{s}) = 0.6144$, or more than half a least significant bit.

While the integer count is still essentially equal at the cycle time registers 206, 210 of the transmitting and receiving nodes 200, 202, the instantaneous edges of each register's shift can differ by up to 0.6144 of bit time, or

10 $(0.6144) / (24.576 \text{ MHz}) = 25 \text{ ns}$.

Even with perfect phase-locked loop circuits in the rest of the clock recovery circuitry, 25ns of jitter can occur.

The second problem associated with jitter arises from the finite length nature of the generated time stamps and the resulting quantization noise. This
15 quantization noise is correlated to the PHY clock circuit 216 and the generated time stamp period of the transmitting node 200. When the receiving node 202 recovers the sample rate clock signal from the time stamp information, this clock is jittered by the quantization error. When this jittered clock is used to drive either a digital-to-analog or analog-to-digital converter, unwanted distortion is introduced into the converted
20 audio signal and degrades signal quality.

SUMMARY

In accordance with the present invention, a method is provided for recovering sample clock signals. The method is performed in connection with a

system including an isochronous device, with the isochronous device having a stored cycle time value that is set by a periodic command issued at times referenced to a first clock signal. The method includes producing a second clock signal referenced to the first clock signal, and incrementing the stored cycle time value in response to the second clock signal. A time stamp value is extracted from a data packet received by the isochronous device. The time stamp value is then compared to the stored cycle time value, and a pulse signal is produced in the event of a match. The frequency of the sample clock signal is then proportional to the frequency of successive pulses. The method may be performed in connection with an isochronous communications bus, such as an IEEE 1394 bus. In such case, the periodic command may be the cycle start command issued by the cycle master, with the first clock signal being produced by the cycle master. The second clock may then be referenced to the incrementing of the cycle-count field of the stored cycle time value.

In accordance with another aspect of the present invention, circuitry is provided for receiving a stream of data packets having associated time stamp values. The circuitry includes a buffer for receiving and temporarily storing the data packets. A packet parser is coupled with the buffer and separates the time stamp values from the data packets. A clock recovery circuit is coupled with the packet parser and compares the time stamp values to a cycle time value, with the clock recovery circuit then producing a data sample clock signal referenced to matched comparisons. A cycle time register is coupled with the clock recovery circuit and provides the cycle time value, which is set in response to a periodic command and incremented in response to a clocking signal. A clocking circuit is coupled with the cycle time register and provides the clocking signal, which is referenced to the periodic command. The circuitry may further include a phase-locked loop circuit that drives the clocking circuit, with the phase-locked loop circuit being referenced to the periodic command. The circuitry may be adapted for coupling with an isochronous

communications bus, such as an IEEE 1394 bus. In such case, the periodic command may be the cycle start command issued by the cycle master, with the clocking signal then referenced to the incrementing of the cycle-count field of the stored cycle time value.

5 In accordance with a further aspect of the invention, a method is provided for generating a time stamp value referenced to a data sample clock for transmission with an isochronous data packet. The method includes latching a cycle time value at a time referenced to the data sample clock, adding a dither value, and filtering the result. The dither value may be determined according to a triangular
10 probability density function, and the filtering may include shifting noise out of the frequency range of the data sample clock.

In accordance with yet another aspect of the invention, circuitry is provided for transmitting a stream of data packets having associated time stamp values. The circuitry includes a cycle time register that provides a cycle time value.
15 The cycle time value is incremented by a clocking signal provided by a clocking circuit. A data interface provides data and a corresponding data sample clock signal. A time stamp generator is coupled with the data interface and with the cycle time register. The time stamp generator produces the time stamp values by latching cycle time values at times referenced to the data sample clock, adding dither values, and
20 filtering the resulting sum values. A packet generator is coupled with the data interface and with the time stamp generator. The packet generator combines the time stamp values with the data to form data packets. The circuitry may further include a packet buffer for temporarily storing data packets received from the packet generator. The packet buffer may be coupleable with an isochronous communications bus, such
25 as an IEEE 1394 bus, for transmission of the data packets thereon.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a functional block diagram that depicts a typical IEEE 1394 system.

Figure 2 is a functional block diagram that depicts circuitry for producing time stamps by a prior art transmitting device and circuitry for sample rate clock recovery in a prior art receiving device in an IEEE 1394 system.

Figure 3 is a functional block diagram depicting a received isochronous datapath through interface circuitry in accordance with an embodiment of the present invention.

Figure 4 is a functional block diagram depicting a transmit isochronous datapath through interface circuitry in accordance with another embodiment of the present invention.

Figure 5 is a functional block diagram depicting circuitry included in the interface of Figure 4 for decorrelating and reducing noise in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

The following is a description of circuitry and methods for reducing jitter in a recovered data sample clock. The circuitry and methods are conformable to the applicable IEEE 1394, ISO/IEC 13213, and IEC 61883 standards. In this description, certain details are set forth in order to provide a thorough understanding of various embodiments of the present invention. It will be clear to one skilled in the art, however, that the present invention may be practiced without these details. In other instances, well-known circuits, circuit components, control signals, and timing and communications protocols have not been shown or described in detail in order to

avoid unnecessarily obscuring the description of the various embodiments of the invention. The described subject matter relates to technology similar to that disclosed in a concurrently filed patent application, entitled "Method and Apparatus for Data Sample Clock Recover," the disclosure of which is incorporated herein by
5 reference.

Figure 3 depicts an embodiment of the invention that addresses the above-identified first problem associated with jitter in prior art approaches to isochronous communications. Figure 3 shows certain circuitry included within a Link layer 300 of interface circuitry coupling the 1394 bus 102 to an application host
10 302. The figure also depicts a physical/electrical interface or PHY layer 304. The particular circuitry shown within the Link layer 300 is a simplified depiction of the datapath for received isochronous data, together with certain associated control/monitor circuitry. Those skilled in the art will appreciate that a wide variety of circuitry is not shown in Figure 3, such as bus management layer circuitry,
15 transaction layer circuitry, datapath and control circuitry for transmitted isochronous data, and other link layer circuitry associated with asynchronous data protocols. Such well-known circuitry is not shown in order to avoid unnecessarily obscuring the description of embodiments of the present invention.

The Link layer circuitry 300 includes a FIFO 306 for receiving
20 incoming isochronous data packets, such as audio data packets. These data packets are passed on to a packet parser 308 that separates the audio data from the header of the packet, including the time stamp. The audio data is then passed on to another FIFO 310, and then on to the application host 302 via a digital audio interface 312.

The packet parser 308 provides the time stamp values from the
25 isochronous data packets to a sample clock recovery circuit 314. The sample clock recovery circuit 314 includes circuitry like the comparator 212 and the phase-locked

loop 214 described above in connection with Figure 2. The sample clock recovery circuit 314 produces a sample rate clock signal corresponding to the received time stamps and the value stored in a local cycle time register 316. This recovered clock signal is applied to a clocks generator circuit 318, which in turn provides the various
5 well-known clocking signals applied to the digital audio interface 312.

The cycle time register 316 is incremented in response to a local PHY clock 320. Instead of being driven by a quartz crystal, as in the prior art, the PHY clock 320 is instead driven by a phase-locked loop (PLL) circuit 322 that is referenced to a cycle-out pin 324 of the Link layer interface. As is known to those
10 skilled in the art, the cycle-out pin 324 toggles each time the cycle-offset field (lowest 12 bits) of the cycle time register wraps to zero (every 125 μ s) and the cycle-count field (next 13 bits) is correspondingly incremented. Since the cycle-count interval equals the cycle master's cycle start command time interval, the cycle-out pin 324 toggles at a rate proportional to the cycle master's clock (albeit with the above-
15 described jitter). Providing the PLL 322 with a sufficiently large loop time constant will then substantially filter out jitter and produce a clock signal of substantially the same frequency as the cycle master PHY clock. Even if the jitter is not completely filtered, an improved performance still results, since the jittery clock signal produced by the PLL-driven PHY clock will be statistically closer in frequency to the cycle
20 master than the prior art quartz-driven PHY clock. Although depicted as external, those skilled in the art will appreciate that the PLL 322 can be advantageously integrated within either the Link layer 300 or the PHY layer 304.

Each of the circuits described in connection with Figure 3 is of a type well known in the art. One skilled in the art would be able to implement such circuits
25 or their equivalent in the described or equivalent configuration to practice the present invention. Accordingly, internal and operational details of such circuits need not be provided.

Figure 4 depicts an embodiment of the invention that addresses the above-identified second problem associated with jitter in prior art approaches to isochronous communications. Figure 4 shows circuitry included within a Link layer 400 of interface circuitry coupling the 1394 bus 102 to an application host 402. The figure also depicts a physical/electrical interface or PHY layer 404. The particular circuitry shown within the Link layer 400 is a simplified depiction of the datapath for isochronous data to be transmitted via the 1394 bus 102, together with certain associated control/monitor circuitry. Those skilled in the art will appreciate that a wide variety of circuitry is not shown in Figure 4, such as bus management layer circuitry, transaction layer circuitry, datapath and control circuitry for received isochronous data, and other link layer circuitry associated with asynchronous data protocols. Such well-known circuitry is not shown in order to avoid unnecessarily obscuring the description of embodiments of the present invention.

The Link layer circuitry 400 includes a digital audio interface 406 that receives incoming audio data from the application host 402 and passes this data on to a FIFO 408. This audio data is passed on to a packet generator 410 that creates an isochronous data packet, including the audio data and a time stamp. The data packet is passed on to another FIFO 412, and then transmitted via the 1394 bus 102 to a receiving device.

The packet generator 410 receives the time stamp values from a time stamp generator circuit 414, which is discussed in further detail below. The time stamps correspond with values received from a local cycle time register 416 at times referenced to the audio sample clock signal received from the digital audio interface 406. The cycle time register 416 may be clocked conventionally or as described above in connection with Figure 3.

Figure 5 depicts certain circuitry included in the time stamp generator circuit circuit 414. A time stamp is first produced by conventional time stamp circuitry 500 similar to that described above in connection with the prior art transmitting node 200 of Figure 2. A summation circuit 502 then adds the
5 conventionally generated time stamp value to a dither signal, such as from a triangular probability density function (TPDF) generator 504. As is known to those skilled in the art, dithering the time stamp decorrelates the jitter, at the expense of introducing broadband noise. Feeding back the summation circuit's output through a suitable noise shaping filter 506 then shifts this noise out of the expected frequency
10 band of the sample clock signal to be recovered. Remaining jitter power will then be further reduced during normal filtering done during clock recovery at the receiving node.

Each of the circuits described in connection with Figures 4 and 5 is of a type well known in the art. One skilled in the art would be able to implement such
15 circuits or their equivalent in the described or equivalent configuration to practice the present invention. Accordingly, internal and operational details of such circuits need not be provided.

From the foregoing, it will be appreciated that, although specific embodiments of the invention have been described above for purposes of illustration,
20 various modifications may be made to these embodiments without deviating from the spirit and scope of the invention. While the discussion has been primarily directed to recovering low jitter sample clocks for audio data in IEEE 1394 bus-based systems, the inventive teachings are also applicable to other isochronous communications. Those skilled in the art will understand that any of a wide variety of circuit topologies
25 could be employed to reduce jitter in recovered data sample rate clock signals by reducing the frequency difference between the various local PHY clocks. Also, those skilled in the art will understand that any of a wide variety of circuit topologies could

be employed to reduce jitter in recovered data sample rate clock signals by dithering and filtering transmitted time stamps. Further, many of the functions of the above-described circuit embodiments could instead be performed in software. Indeed, numerous variations are well within the scope of the invention, and the
5 invention is not limited except as by the appended claims.

CLAIMS

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1. In a system including a plurality of isochronous devices exchanging isochronous data packets having associated time stamp values, a selected one of the isochronous devices producing a first clock signal and issuing a periodic command at times referenced to the first clock signal, the periodic command setting cycle time values stored in the isochronous devices, a method of recovering a data sample rate signal, the method comprising:
- producing a second clock signal referenced to the first clock signal;
 - incrementing the stored cycle time value in response to the second clock signal;
 - extracting a time stamp value included in a received one of the data packets;
 - comparing the extracted time stamp value with the stored cycle time value; and
 - when the received time stamp value equals the stored cycle time value, producing a pulse signal, the frequency of the data sample rate signal being proportional to the frequency of successive pulses.
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2. The method of claim 1 wherein producing the second clock signal includes referencing the second clock signal to the periodic command.
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3. The method of claim 1 wherein the isochronous devices are coupled by an IEEE 1394-based bus, and wherein producing the second clock signal includes referencing the second clock signal to the periodic command, the periodic command being a cycle start command broadcast on the bus.
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4. The method of claim 1 wherein the isochronous devices are coupled by an IEEE 1394-based bus, and wherein producing the second clock signal

3 includes referencing the second clock signal to an incrementing of a cycle-count field
4 of the stored cycle time value.

1 5. In a home entertainment system including an audio source
2 coupled with an audio receiver, the audio source producing a stream of audio data
3 packets having associated time stamp values, and the audio receiver receiving the
4 audio data packets, a cycle time value stored in the audio receiver being set by a
5 periodic command referenced to a first clock signal, a method for the audio receiver
6 to reduce jitter in a recovered data sample clock, the method comprising:
7 producing a second clock signal referenced to the first clock signal;
8 incrementing the stored cycle time value in response to the second
9 clock signal;
10 extracting a time stamp value from one of the audio data packets; and
11 comparing the received time stamp value with the stored cycle time
12 value.

1 6. The method of claim 5 wherein producing the second clock
2 signal includes referencing the second clock signal to the periodic command.

1 7. The method of claim 5 wherein the audio source and audio
2 receiver are coupled by an isochronous communications bus, and wherein producing
3 the second clock signal includes referencing the second clock signal to the periodic
4 command, the periodic command being an isochronous cycle start command
5 broadcast on the bus.

6 8. The method of claim 5 wherein the audio source and audio
7 receiver are coupled by an IEEE 1394-based bus, and wherein producing the second
8 clock signal includes referencing the second clock signal to an incrementing of a
9 cycle-count field of the cycle time value stored in the audio receiver.

1 9. Circuitry for receiving a stream of data packets including
2 associated time stamp values, the circuitry comprising:
3 a buffer operable to receive and temporarily store the data packets;
4 a packet parser coupled with the buffer and operable to separate the
5 time stamp values from the data packets;
6 a comparison circuit coupled with the packet parser, the comparison
7 circuit operable to receive the time stamp values and compare the time stamp values
8 to a cycle time value;
9 a cycle time register coupled with the comparison circuit and operable
10 to provide the cycle time value, the cycle time value being set in response to a
11 periodic command, and the cycle time value being incremented in response to a
12 clocking signal; and
13 a clocking circuit coupled with the cycle time register and operable to
14 provide the clocking signal, the clocking signal being referenced to the periodic
15 command.

1 10. The circuitry of claim 9 wherein the circuitry is operable to be
2 coupled to an IEEE 1394-based bus, and wherein the periodic command is a cycle
3 start command broadcast on the bus.

1 11. The circuitry of claim 9, further comprising a phase-locked loop
2 circuit coupled with and driving the clocking circuit, the phase-locked loop being
3 referenced to the periodic command.

1 12. The circuitry of claim 9 wherein the circuitry is operable to be
2 coupled to an isochronous communications bus, and further comprising a
3 phase-locked loop circuit coupled with and driving the clocking circuit, the

- 4 phase-locked loop being referenced to the periodic command, the periodic command
5 being an isochronous cycle start command broadcast on the bus.

1 13. The circuitry of claim 9 wherein the circuitry is operable to be
2 coupled to an IEEE 1394-based bus, and further comprising a phase-locked loop
3 circuit coupled with and driving the clocking circuit, the phase-locked loop being
4 referenced to an incrementing of a cycle-count field of the cycle time value stored in
5 the cycle time register.

1 14. A home entertainment system comprising audio/video sources
2 coupled with audio/video receivers, the sources each operable to produce a stream of
3 data packets having associated time stamp values, and the receivers each operable to
4 receive a selected one of the streams of data packets, at least one of the receivers
5 comprising:

6 a buffer operable to receive and temporarily store the received data
7 packets;

8 a packet parser coupled with the buffer and operable to separate the
9 time stamp values from the data packets;

10 a clock recovery circuit coupled with the packet parser, the clock
11 recovery circuit operable to receive the time stamp values and compare the time
12 stamp values to a cycle time value, the clock recovery circuit operable to produce a
13 data sample clock signal referenced to matched comparisons of the time stamp values
14 and the cycle time value;

15 a cycle time register coupled with the clock recovery circuit and
16 operable to provide the cycle time value, the cycle time value being set in response to
17 a periodic command, and the cycle time value being incremented in response to a
18 clocking signal; and

19 a clocking circuit coupled with the cycle time register and operable to
20 provide the clocking signal, the clocking signal being referenced to the periodic
21 command.

1 15. The home entertainment system of claim 14 wherein the
2 audio/video sources are coupled with the audio/video receivers by an isochronous
3 communications bus, and wherein wherein the periodic command is an isochronous
4 cycle start command broadcast on the bus.

1 16. The home entertainment system of claim 15 wherein the
2 isochronous communications bus is an IEEE 1394 bus.

1 17. The home entertainment system of claim 14 wherein the one
2 receiver further comprises a phase-locked loop circuit coupled with and driving the
3 clocking circuit, the phase-locked loop being referenced to the periodic command.

1 18. The home entertainment system of claim 14 wherein the
2 audio/video sources are coupled with the audio/video receivers by an isochronous
3 communications bus, and wherein the one receiver further comprises a phase-locked
4 loop circuit coupled with and driving the clocking circuit, the phase-locked loop
5 being referenced to the periodic command, the periodic command being an
6 isochronous cycle start command broadcast on the bus.

1 19. The home entertainment system of claim 14 wherein the
2 audio/video sources are coupled with the audio/video receivers by an IEEE 1394 bus,
3 and wherein the one receiver further comprises a phase-locked loop circuit coupled
4 with and driving the clocking circuit, the phase-locked loop being referenced to an
5 incrementing of a cycle-count field of the cycle time value stored in the cycle time
6 register.

1 20. A method of generating a time stamp value referenced to a data
2 sample clock for transmission with an isochronous data packet, the method
3 comprising:

4 latching a cycle time value at a time referenced to the data sample
5 clock;

6 adding a dither value to the cycle time value; and
7 filtering the addition of the dither value and the cycle time value.

1 21. The method of claim 20 wherein adding a dither value includes
2 adding a value determined according to a triangular probability density function.

1 22. The method of claim 20 wherein filtering includes shifting noise
2 out of the frequency range of the data sample clock.

1 23. A method of reducing jitter in a data sample clock recovered
2 from a stream of data packets, comprising:
3 generating a time stamp;
4 dithering the time stamp;
5 filtering the the dithered time stamp; and
6 transmitting the dithered and filtered time stamp along with an
7 associated one of the data packets.

1 24. The method of claim 23 wherein dithering the time stamp
2 includes dithering the time stamp according to a triangular probability density
3 function.

1 25. The method of claim 23 wherein filtering the time stamp
2 includes shifting noise out of an expected frequency range of the recovered data
3 sample clock.

1 26. The method of claim 23 wherein dithering the time stamp
2 includes adding a dither value to the time stamp.

1 27. The method of claim 26 wherein filtering the dithered time
2 stamp includes feeding back the dithered time stamp.

1 28. Circuitry for transmitting a stream of data packets including
2 associated time stamp values, the circuitry comprising:
3 a cycle time register operable to provide a cycle time value, the cycle
4 time value being incremented in response to a clocking signal;
5 a clocking circuit coupled with the cycle time register and operable to
6 provide the clocking signal;
7 a data interface operable to provide data and a corresponding data
8 sample clock;
9 a time stamp generator coupled with the data interface and with the
10 cycle time register, the time stamp generator operable to latch cycle time values at
11 times referenced to the data sample clock, the time stamp generator further operable
12 to add dither values to the latched cycle time values, to filter the resulting sum values,
13 and to correspondingly produce the time stamp values; and
14 a packet generator coupled with the data interface and with the time
15 stamp generator, the packet generator operable to combine the time stamp values with
16 the data to form the data packets.

1 29. The circuitry of claim 28, further comprising a packet buffer
2 coupled with the packet generator and operable to receive and temporarily store the
3 data packets, the packet buffer operable to be coupled with an isochronous
4 communications bus for transmission of the data packets thereon.

1 30. The circuitry of claim 29 wherein the isochronous
2 communications bus is an IEEE 1394 bus.

1 31. A home entertainment system comprising audio/video sources
2 coupled with audio/video receivers, the sources each operable to produce a stream of
3 data packets having associated time stamp values, and the receivers each operable to
4 receive a selected one of the streams of data packets, at least one of the transmitters
5 comprising:

6 a cycle time register operable to provide a cycle time value, the cycle
7 time value being incremented in response to a clocking signal;

8 a clocking circuit coupled with the cycle time register and operable to
9 provide the clocking signal;

10 a data interface operable to provide data and a corresponding data
11 sample clock;

12 a time stamp generator coupled with the data interface and with the
13 cycle time register, the time stamp generator operable to latch cycle time values at
14 times referenced to the data sample clock, the time stamp generator further operable
15 to add dither values to the latched cycle time values, to filter the resulting sum values,
16 and to correspondingly produce the time stamp values; and

17 a packet generator coupled with the data interface and with the time
18 stamp generator, the packet generator operable to combine the time stamp values with
19 the data to form the data packets.

1 32. The home entertainment system of claim 31 wherein the
2 audio/video sources are coupled with the audio/video receivers by an isochronous
3 communications bus.

1 33. The home entertainment system of claim 32 wherein the
2 isochronous communications bus is an IEEE 1394 bus.

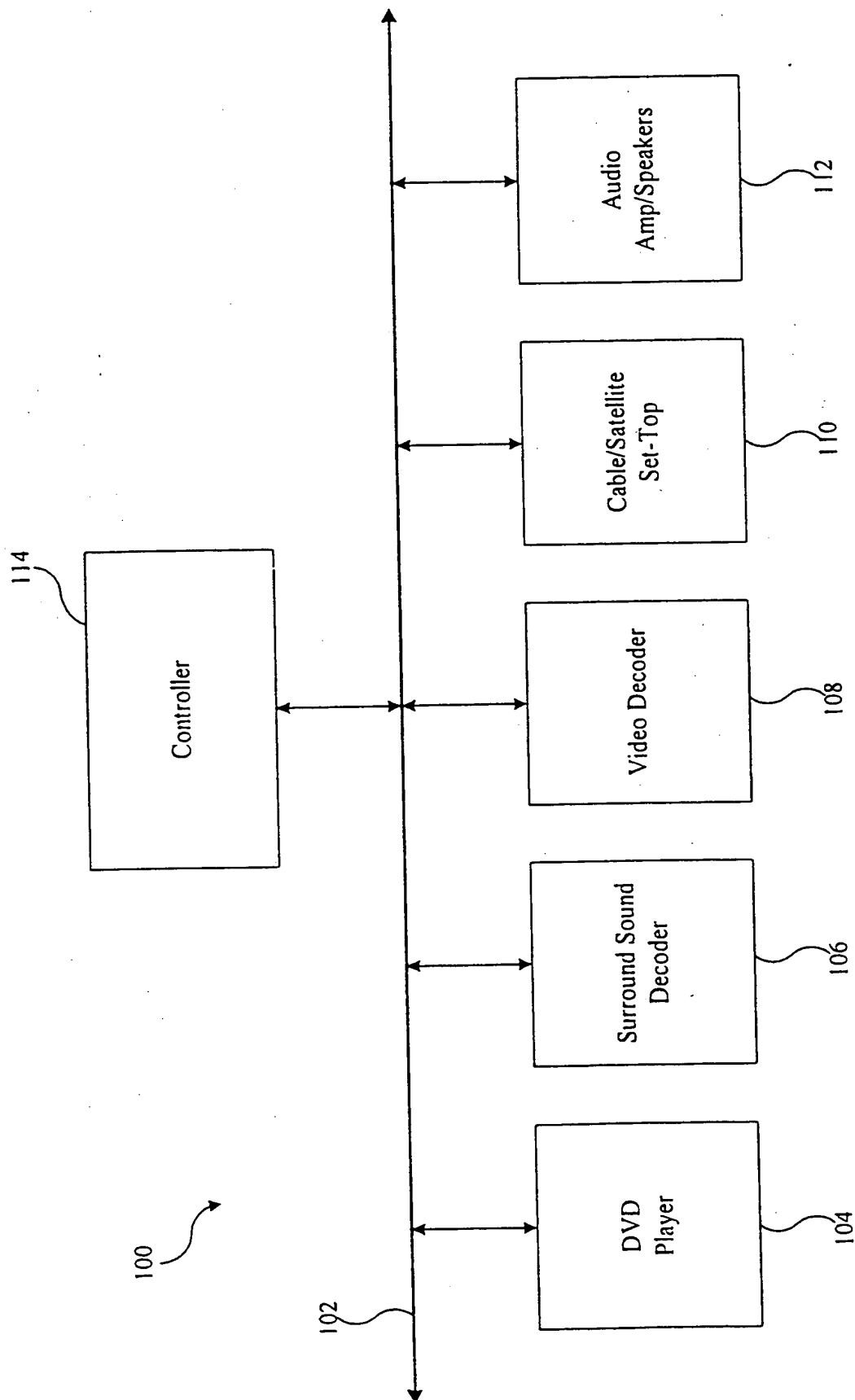


Fig. 1

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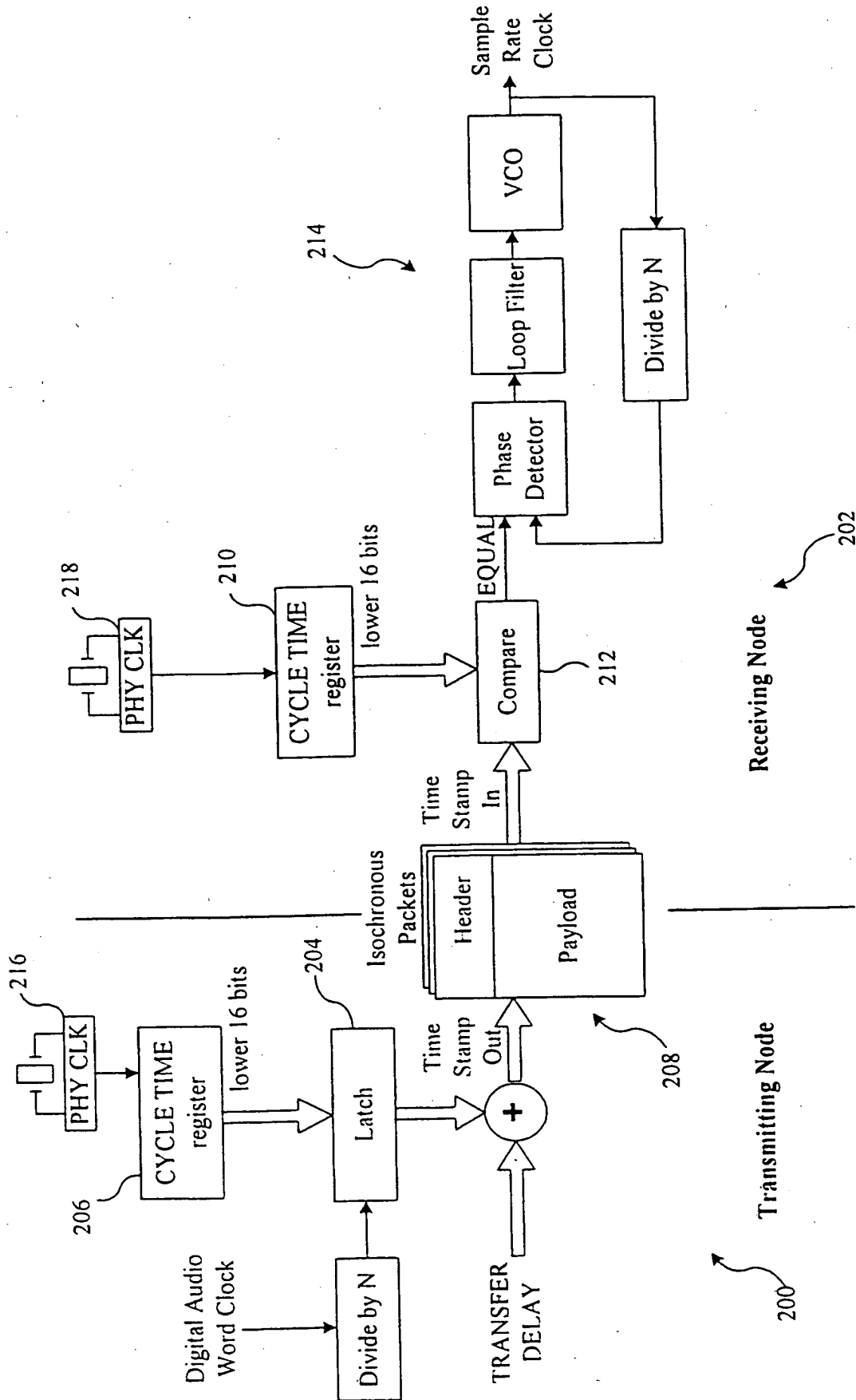
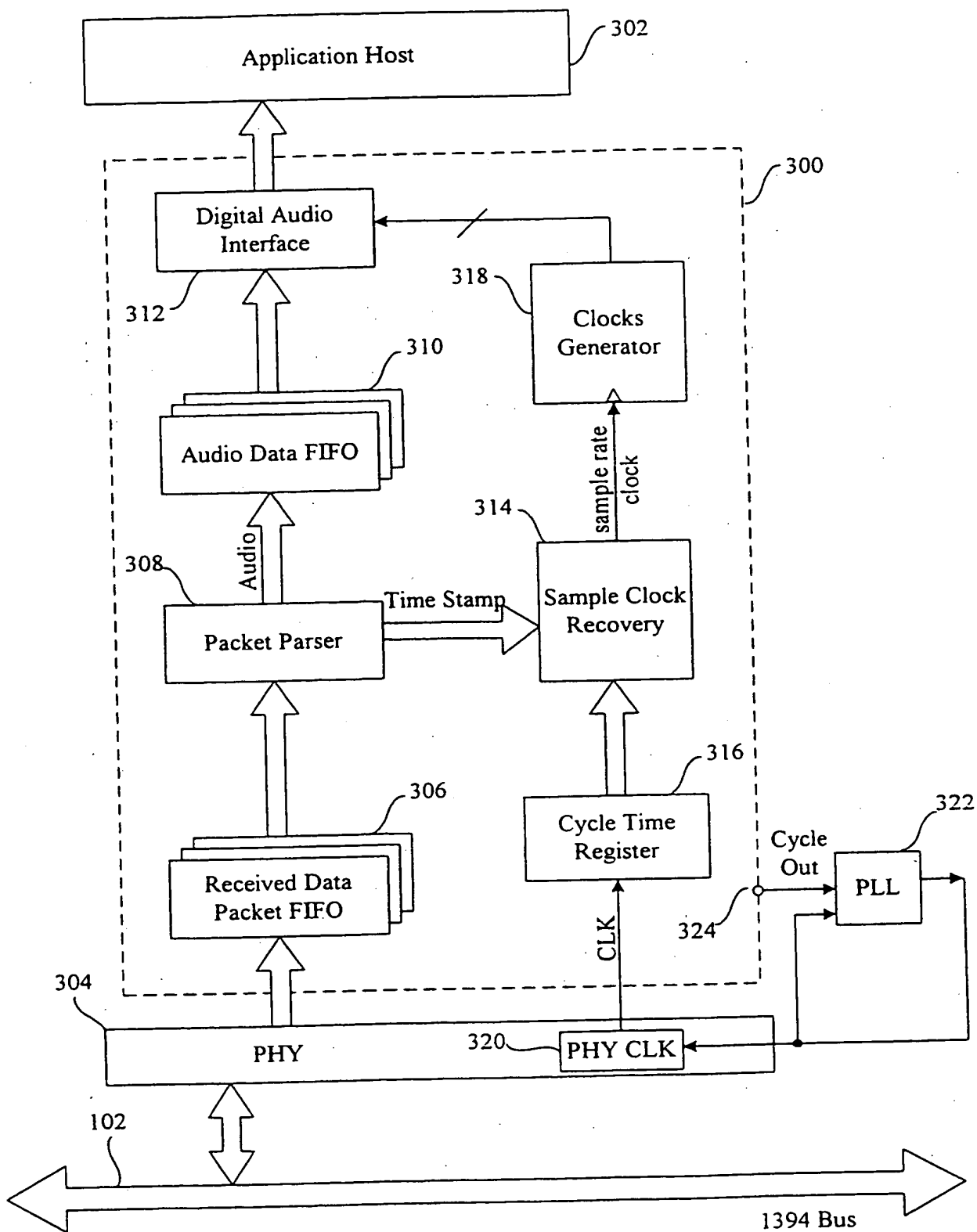
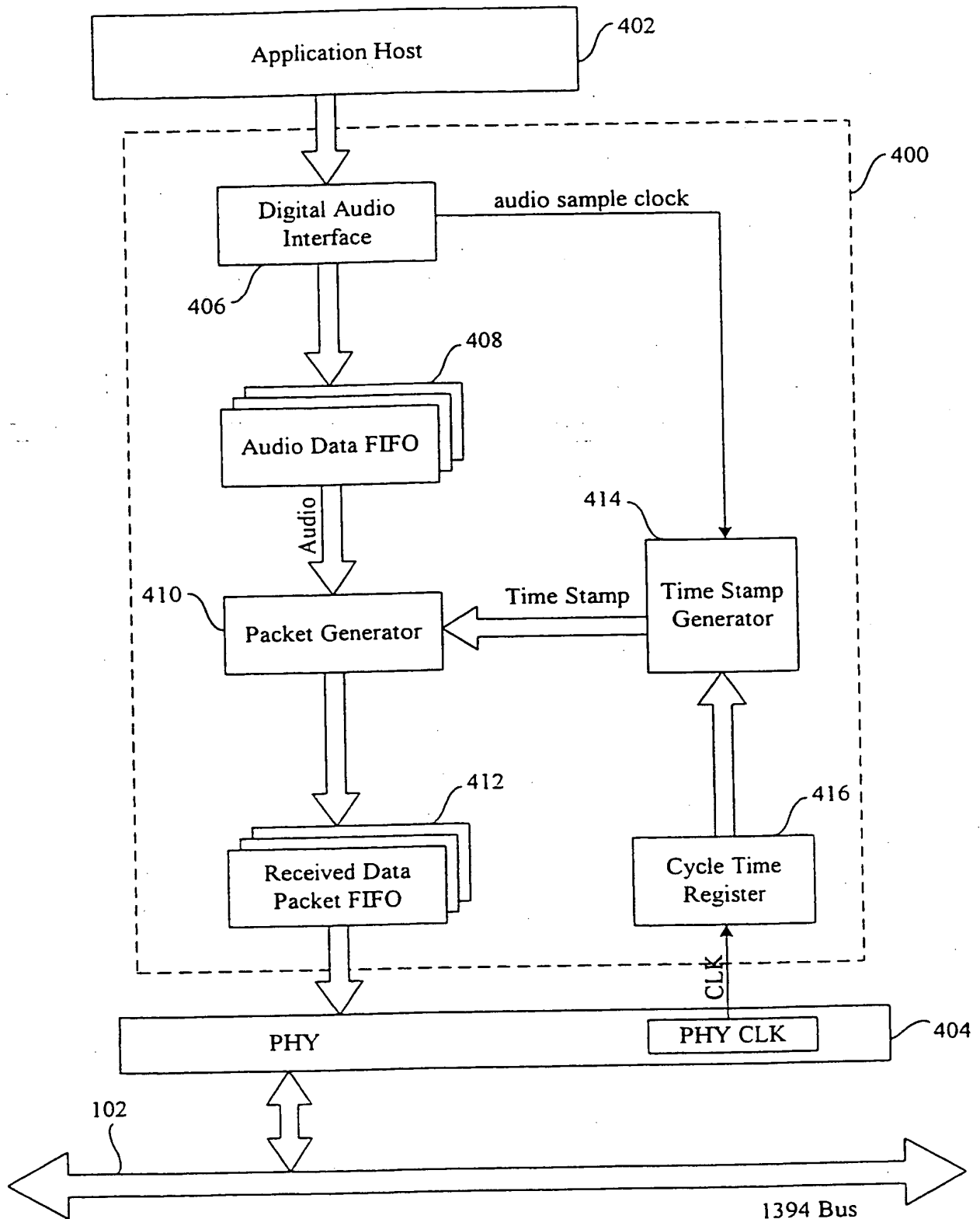
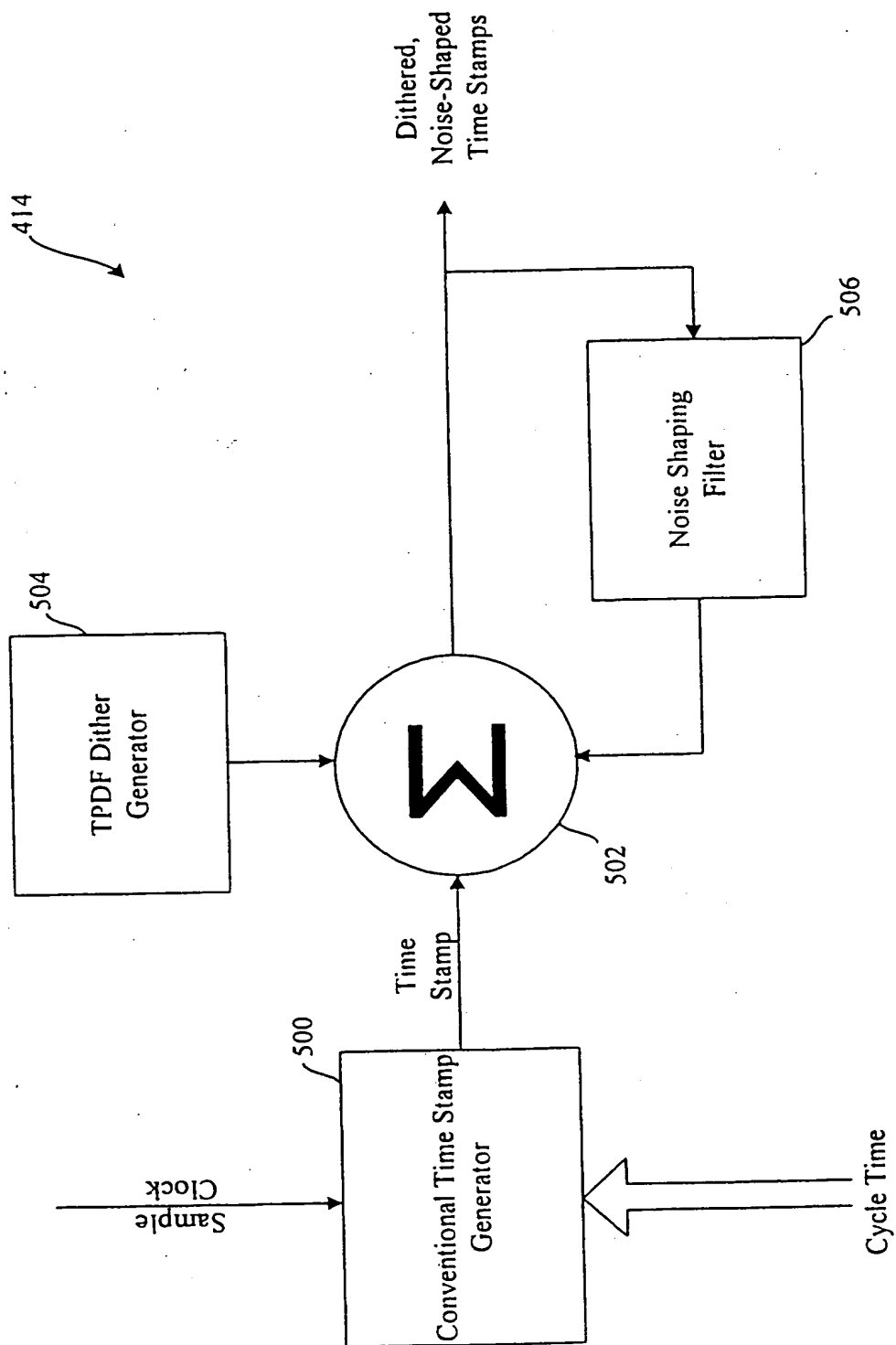


Fig. 2 (Prior Art)

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**Fig. 3**

**Fig. 4**

*Fig. 5*



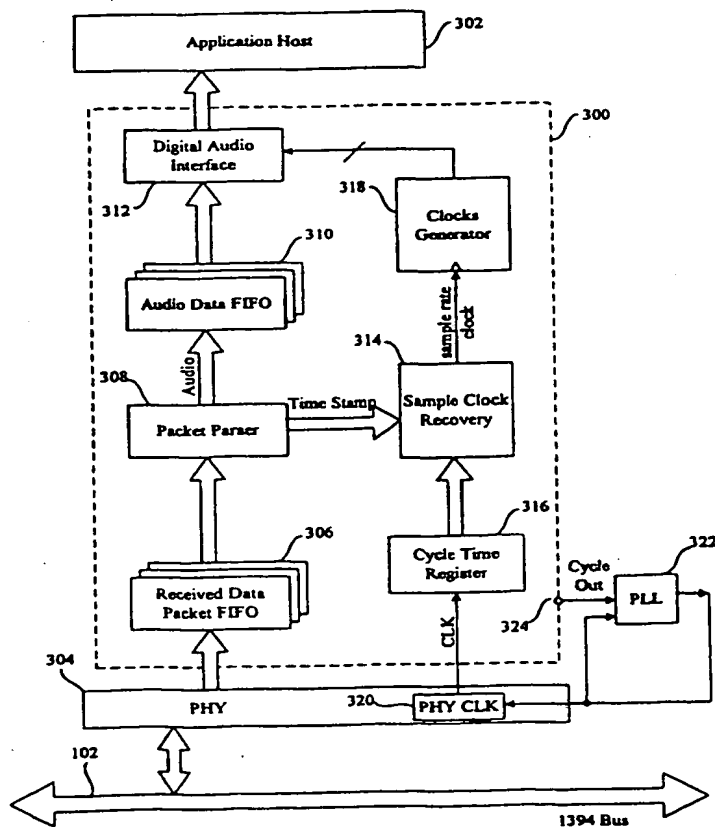
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(54) Title: METHOD AND APPARATUS FOR LOW JITTER CLOCK RECOVERY

(57) Abstract

A method and apparatus is described for reducing jitter in data sample clock rates recovered from isochronous streams of data packets having associated time stamp values, such as in an IEEE 1394 bus-interconnected system. Jitter associated with variations in the free running quartz-driven PHY clocks is reduced by instead driving local PHY clocks with a phase-locked loop circuit referenced to the Link cycle-out pin, which toggles when the cycle time register cycle-offset field wraps and the cycle-count field increments. Because the cycle-out pin toggles at a frequency proportional to the cycle master's PHY clock, jitter associated with local PHY clock variations is reduced. Jitter associated with quantization noise from finite length time stamp generation is reduced by dithering and noise shape filtering conventional time stamps. This decorrelates the jitter and shifts the associated noise out of the expected frequency band of the sample clock signal to be recovered.



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International Application No.

PCT/US 99/10226

A. CLASSIFICATION OF SUBJECT MATTER

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G06F H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|------------|---|---|
| X | EP 0 838 926 A (SONY CORP) 29 April 1998 (1998-04-29) | 1, 5, 9, 14, 20, 23, 28, 31 |
| A | column 5, line 30 -column 8, line 9 | 2-4, 6-8, 10-13, 15-19, 21, 22, 24-27, 29, 32-34 |
| A | abstract; claims 1-3; figures 1, 4 | |
| | EP 0 695 063 A (SONY CORP) 31 January 1996 (1996-01-31) | 1-34 |
| | column 1, line 40 -column 2, line 24 column 7, line 12 -column 9, line 54 column 10, line 24 -column 12, line 11 abstract; claims 1-9; figures 1-3 | |
| | -/- | |

☒ Further documents are listed in the continuation of box C.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|------------|---|--|
| A | <p>US 5 526 362 A (AHMED HASSAN ET AL) 11 June 1996 (1996-06-11)</p> <p>column 1, line 21 -column 2, line 37 column 2, line 55 -column 4, line 12 abstract; figure 2</p> | <p>1, 5, 9, 14, 20, 23, 28, 31</p> |

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 99/10226

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
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